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EE/EX-403-CBGS

B.Tech., IV Semester

Examination, June 2020

Choice Based Grading System (CBGS)

Digital Electronics and Logic Design (DELD)

Time : Three Hours

Maximum Marks : 70

Note: i) Attempt any five questions.

ii) All questions carry equal marks.

iii) In case of any doubt or dispute the English version question should be treated as final.

1. a) Minimize the following function using K-map and realize using logic gates: 7

   F (A, B, C, D) = Σm (1, 5, 7, 13, 15) + d (0, 6, 12, 14)

   K-map

   logic

   F (A, B, C, D) = Σm (1, 5, 7, 13, 15) + d (0, 6, 12, 14)

   b) State and prove De-Morgan's theorem. Also prove the following rules of Boolean algebra: 7

   i) A+A' B = A + B

   ii) (A + B) (A + C) = A+BC

De-Morgan's theorem

i) A+A'B = A + B

ii) (A + B) (A + C) = A+BC

2. a) Do the following conversions: 7

i) $(101110.0101)_2 \rightarrow (\ )_8$

ii) $(432A)_{16} \rightarrow (\ )_2$

iii) $(428.10)_{10} \rightarrow (\ )_2$

b) Using K-map convert the following standard POS expression into a minimum POS expression, standard SOP expression and minimum SOP expression. 7

K-map POS

POS SOP SOP

A{^ì¶{³V '| n[ad{V©V H$a| :

(A'+B+C+D) (A+B'+C+D) (A+B+C+D') (A+B+C'+D') (A'+B+C+D') (A+B+C'+D).

3. a) How will you implement full-adder using half-adder? Explain the circuit diagram. 7

lf-adder full-adder

b) Implement the following expression using 8 to 1 multiplexer: 7

F (A, B, C, D) =Σm (0, 3, 4, 7, 8, 9, 13, 14)

8 to 1

F (A, B, C, D) =Σm (0, 3, 4, 7, 8, 9, 13, 14)

4. a) Draw and explain the look ahead carry generator. 7

Look ahead carry generator

b) What is race around condition? Explain with the help of timing diagram. How is it removed in basic flip-flop circuit? 7

Race around condition (Timing diagram)

¡ ?

5. a) Design sequence generator using J-K Flip-Flop for the following sequence: 7

1 → 3 → 5 → 6 → 7 → 1.

sequence go

sequence generator

1 → 3 → 5 → 6 → 7 → 1.

b) Explain the difference between asynchronous and synchronous counter. How lockout condition in counter is avoided? 7

'| lockout condition

6. a) Explain with neat diagram working of serial- in serial-out 4-bit shift register. Draw necessary timing diagram. 7

serial- in serial-out 4-bit shift register

b) Draw and explain : 7

i) Johnson Counter

ii) BCD Counter

7. a) Draw the basic structure of CPLD. Explain its features in brief. 7

b) Explain analog to digital conversion using successive approximation. 7

Successive approximation

8. Write short notes on (any two): 14

a) PAL

b) Master-slave FF

c) ROM

d) Applications of sequential circuits

A) PAL

~) Master-slave FF

g) ROM

X) Sequential Circuits

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